

COMPUTER FOR EXECUTING TWO DIFFERENT INSTRUCTION SETS

ABSTRACT

A computer. A processor pipeline alternately executes instructions coded for first and second different computer architectures or coded to implement first and second different processing conventions. A memory stores instructions for execution by the processor pipeline, the memory being divided into pages for management by a virtual memory manager, a single address space of the memory having first and second pages. A memory unit fetches instructions from the memory for execution by the pipeline, and fetches stored indicator elements associated with respective memory pages of the single address space from which the instructions are to be fetched. Each indicator element is designed to store an indication of which of two different computer architectures and/or execution conventions under which instruction data of the associated page are to be executed by the processor pipeline. The memory unit and/or processor pipeline recognizes an execution flow from the first page, whose associated indicator element indicates the first architecture or execution convention, to the second page, whose associated indicator element indicates the first architecture or execution convention. In response to the recognizing, a processing mode of the processor pipeline or a storage content of the memory adapts to effect execution of instructions in the architecture and/or under the convention indicated by the indicator element corresponding to the instruction's page.

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